REMARKS/ARGUMENTS

Claims 1 and 12 have been amended to improve the form thereof as suggested by the Examiner.

Claim 5 has been canceled.

Responsive to the rejection of claims under 35 U.S.C. §112, first and second paragraphs, it should be noted the subject matter that is allegedly not disclosed consistent with paragraphs one and two was disclosed in the parent application. The Examiner has stated that the "fact that the subject matter of the rejected claims was disclosed in the original claims in the parent application does not mean that there is support in the drawings and there is adequate description in the disclosure for the claimed limitations, as recited in claims 1, 12 and 27". The Examiner is in error.

It is well known in U.S. patent practice that original claims are considered part of the original disclosure. MPEP §2163.06, III. Furthermore, a continuation application enjoys the benefit of the disclosure in the parent application. MPEP §2163.03, II.

In addition, the burden of proving lack of adequate disclosure is on the Examiner. MPEP §2163.04. The Examiner must set forth facts to establish a "reasonable basis" for rejecting claims based on section 112. See MPEP §2163.04.

The Office Action does not include any facts, but only conclusory statements. Thus, the rejections as set forth in the Office Action are without adequate foundation.

Moreover, it is very clear from the specification that the disclosed devices are "vertical conduction" type of devices adapted for flip-mounting. It is well-known that a vertical conduction type of a device includes a conduction path that is vertically oriented with respect to the top surface of the device. Thus, it is submitted that the description adequately discloses the claimed subject matter. Reconsideration is requested.

Regarding claim 27, it is clear that a sinker 90 or bodies 92 can constitute a high conductivity element. It is submitted, therefore, that claim 27 is supported by the specification.

Claims 1, 12 and 27 have been rejected under 35 U.S.C. §103(a) as obvious over Nakagawa et al. (Nakagawa), U.S. 5,105,243, Coe et al. (Coe) U.S. 5,128,730 and Rinne et al. (Rinne) U.S. 6,117,799. Reconsideration is requested.

Claim 1 calls for the following combination:

1. A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced and metallized layers formed on said first major surface and insulated from one another and connected to said P region and said N region respectively; a bottom metallized layer extending across said second major surface; and

a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device, wherein a current path from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

Claim 12 calls for the following combination:

12. A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second coplanar, laterally spaced metallized layers formed on said first major surface and insulated one another and connected to said P region and said N region respectively; a third metallized layer atop said first major surface which is coplanar with and laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row, wherein a current path from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

Claim 27 call for the following combination:

27. A semiconductor device comprising a silicon die having first and second parallel surfaces; a region of one conductivity type extending from said first surface and into the body of said die; a junction pattern defined in said device

formed by a plurality of laterally spaced diffusions of the other conductivity type into said region of one conductivity type; a first conductive power electrode formed atop said first surface and in contact with said plurality of laterally spaced diffusions; a second conductive power electrode formed atop said first surface which is coplanar with and laterally spaced from and insulated from said first conductive electrode and in electrical contact with the body of said die through a high conductivity element located outside said region of one conductivity type; and at least one solder ball connector formed atop each of said first and second conductive electrodes respectively; the current path from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface.

It has been alleged that Nakagawa teaches "a current path from said source electrode to said drain electrode [that] includes a vertical component which is generally perpendicular to said first major surface (since Nakagawa et al. teach an electrode 14 located on the second major surface of the device)".

It is respectfully submitted that the claims should be read carefully. As presently worded the claims call for the current path between the power electrodes (source and drain electrodes) that are on the same surface to have a vertical component. The Examiner alleges that Nakagawa teaches a vertical current path between electrodes on opposite surfaces of a die. Clearly, the limitation in question does not read on Nakagawa. Thus, Nakagawa fails to teach the limitation necessary to establish a *prima facie* case of obviousness. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2007:

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Name of applicant, assignee or Registered Representative

Signature

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Respectfully submitted,

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